Photolithographic Method for Carbon Nanotube Transistor Fabrication

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Conventional research carbon nanotube field effect transistor (CNT-FET) fabrication methods such as electron beam lithography (EBL) have substrate material limitations and low-throughputs. This alternative method for CNT-FET fabrication enables fabrication on totally insulating substrates necessary for high-frequency operation. The large number of devices, in combination with an automated probe station, enables statistical studies of CNT device properties.

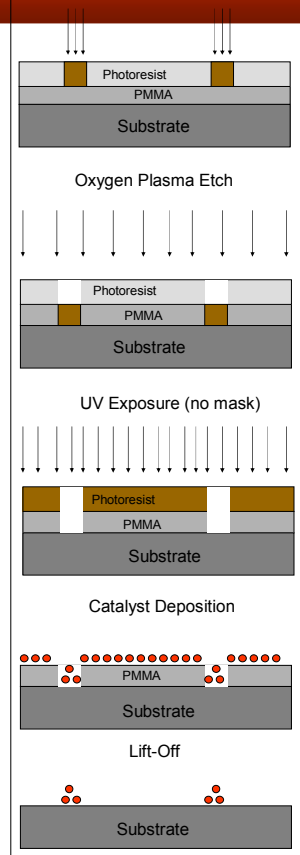


Figure 1. Catalyst patterning steps after A. Ural, Y. Li and H. Dai in Applied Physics Letters Vol. 81, No. 18, pp. 3464.

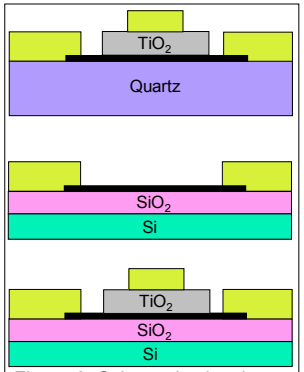
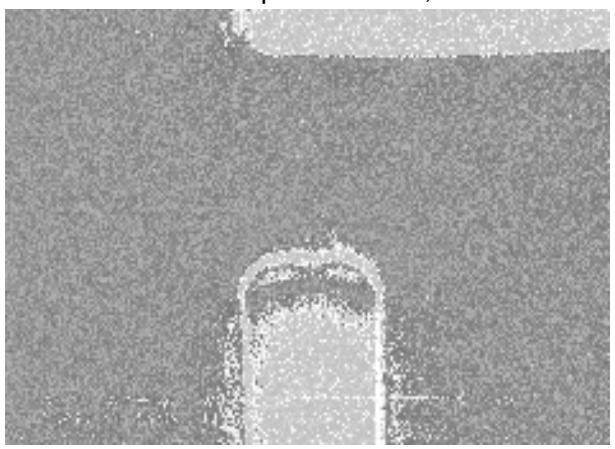
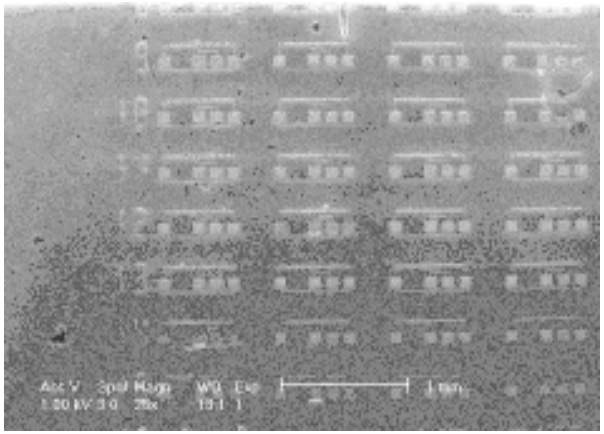
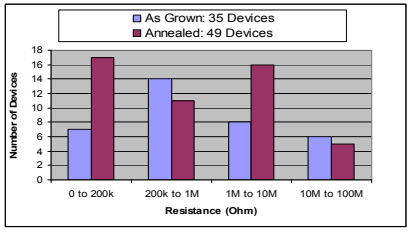


Figure 2. Schematic showing three possible CNT-FET geometries: local top gate (top), global back gate (middle) and dual gate (bottom)





Figures 3 and 4: Scanning Electron Microscope (SEM) images of (Left) An individual CNT-FET device with Si back gate and (Right) part of the device array (180 devices total)



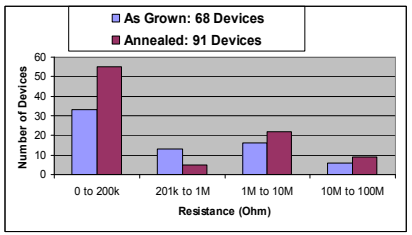


Figure 5. Histograms showing the effect of annealing in hydrogen on device resistances. The number of measurable devices (<100ΩM) increased from 103 to 140.

Features

- Patterned nanotube growth
- Variable channel length (2,4,6,10mm)
- Optional channel processing
- Optional top gate
- Alignment marks for EBL
- Reduces per-device fabrication time from 2 hours to 10 minutes.

Applications

- Statistical process tuning
- CNT devices on insulating substrates.
  - High-Frequency devices
  - Optical devices
- Functionalized CNT devices.
  - Chemical and biological sensors.
- Suspended CNT devices.

Figure 6. Optical microscope picture of a finished top-gated CNT-FET using TiO_2 dielectric on quartz substrate.

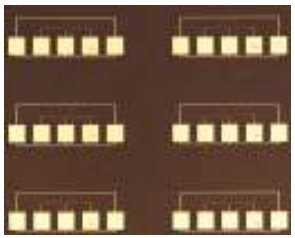


Figure 7. Optical picture showing six devices, part of a 180-device array on a quartz substrate.

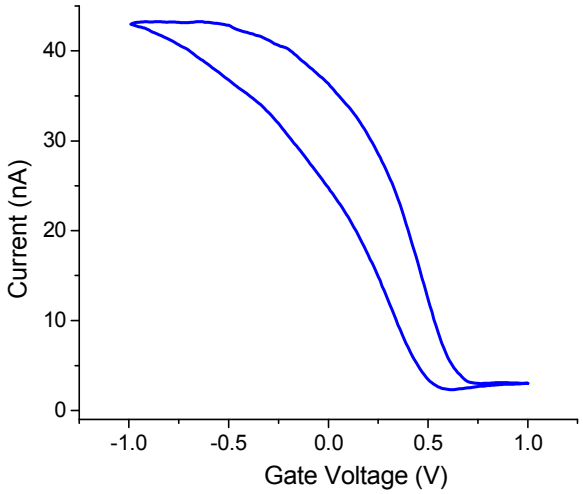


Figure 8. Gate voltage sweep of a top-gated device on quartz using TiO_2 dielectric.